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DESIGN METRICS FOR OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

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Abstract

The primary goal of this thesis work is to offer a design method that will improve the performance of operation transconductance amplifiers (OTAs) in a low power II environment while maintaining low power consumption. It is proposed to increase the performance of the classic Recycling Folded Cascode and Improved Recycling Folded Cascode (IRFC) OTA structures by using an input stage with an asymmetrical current split, in order to achieve this aim. An further strategy for improving the performance of low voltage conventional super class AB RFC OTAs is positive feedback, which is implemented in this paper.

Keywords: *Transconductance, Metrics*

Introduction

The design of an analogue circuit, particularly one that uses little power, is a difficult task to do. The Operational Transcondactance Amplifier, often known as the OTA, is a fundamental component in several analogue integrated circuits, including the ADC, Gm-C filter, and Delta Sigma modulator, among others. The OTA structure is critical in all of these integrated circuits since it determines how well they perform. A number of performance characteristics, including gain bandwidth (GBW), DC gain, Common Mode Rejection Ratio (CMRR), and average power, are taken into consideration while selecting an OTA. A well-designed OTA with better processing characteristics like as speed, power consumption, gain, and GBW is a remarkable achievement in and of themselves. This chapter primarily focuses on the performance characteristics, both theoretically and analytically, that control the design of OTAs and how they are determined. Optimization strategies that are ideal for low voltage and low power applications, particularly at the transistor level, are also covered in this paper. gives a high level overview of essential single stage OTA topologies

Objective

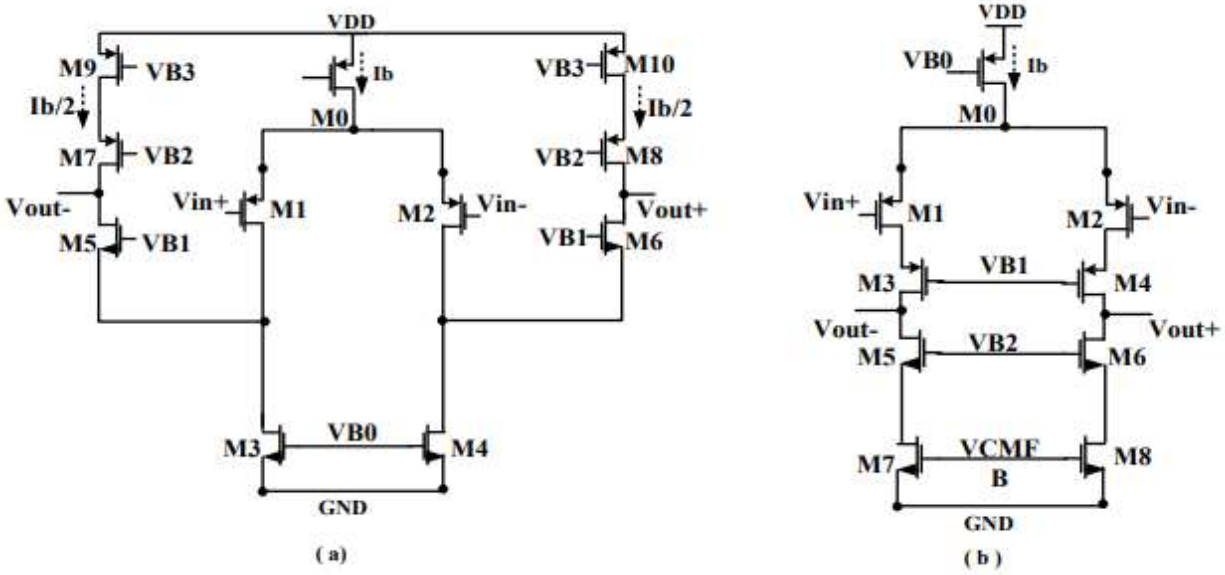
1. Design and simulate OTA structures to validate their performance using available sub-micron CMOS technology.
2. Implementation of the application using the proposed OTA structure making use of available nano-meter CMOS VLSI technology.

Single Stage OTA structure

In order to provide adequate performance within the power and space constraints, it is necessary to select a topology that is tailored to the application in question [20, 25]. This figure shows three key OTA structures, which are the Telescopic, the Folded Cascode (FC), and the Recyclable Folded Cascode (RFC). These structures are the focus of this section. The following topologies are briefly addressed in terms of their performance metrics in relation to the ones previously mentioned:

The Telescopic Optical Telescope (OTA): The Telescopic OTA, which is comparatively the most power-efficient construction, has the best frequency response available. It is also a structure that reflects the least amount of noise input. But despite its benefits, it is the least ideal for low voltage applications because it provides the least amount of headroom for signal swing at the output and because its supply needs are higher than those of the Folded Cascode OTAs (which are also less expensive). Taking everything into perspective, the Telescopic OTA is the ideal choice in systems that demand extremely high speed and low noise performance, as well as in designs in which signal swing is not a key factor to consider.

OTA with Folded Cascode (FC) Since this OTA shares the advantage of a good frequency performance with the Telescopic OTA, albeit with a degraded efficiency and also has the advantage of a decent low voltage performance unaccompanied by additional noise which it shares with the Current Mirror OTA, it serves as a good middle ground OTA.



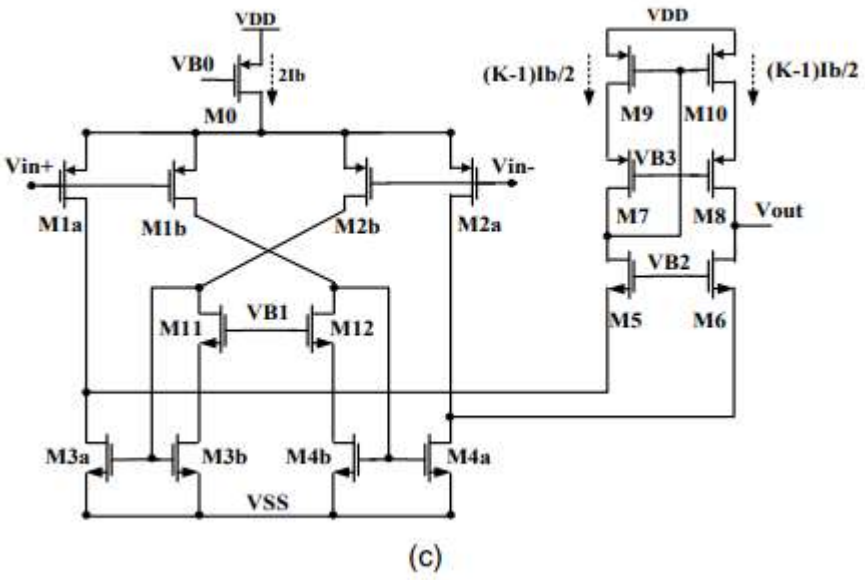


Figure 1.1. (a) Folded cascode OTA (b) Telescopic OTA (c) Recycling Folded Cascode OTA In applications where speed, signal headroom and noise are of significance, the Folded Cascode OTA is most suited, all things being considered. It comes as no surprise therefore, to see the Folded Cascode amplifier being increasingly used either as a single stage, or as the first stage amplifier in a multi-stage amplifier, in the leading-edge designs as well as in literature [42].

Recycling Folded Cascode (RFC) OTA is depicted in Figure 1.1 (c) with the utilization of the PMOS input stage Its development comprises alteration of the current sources at the folding stage by active current mirrors accompanied by a current ratio of 1:K, and being reconnected to a differential pair transistors. It is notable that the consumption of the power is same to the FC OTA for factor K=3. Current mirrors are made more precise and stable by the transistors M11-M12. This configuration boosts the transconductance, GBW and SR of the OTA without increasing current consumption, as folding is produced by active current mirrors with current gain K which scale the signal currents provided by the differential pair [42]. In the next sections, numerous design elements will be explored for Telescopic, FC and RFC OTA. To make this topic simpler, the square law I-V model of MOS devices under saturation will be alluded to frequently. (3.1) is the equation used to represent this. In this equation, μN, Cox, W, L, VGS, VT and VGST are respectively the electron mobility, gate oxide per unit area, width, length, gate-source, threshold, and overdrive voltages

$$I_{D0} = \frac{1}{2}\mu_N C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 = \frac{1}{2}\mu_N C_{ox}\frac{W}{L}V_{GST}^2$$

Whereas this model disregards multiple second order effects that are part of and serve as a model for the leading-edge CMOS technologies, it performance is a close estimation of a MOS device. However, as needed and where relevant, secondary order effects will be shown.

LITERATURE REVIEW

A low-power circuit designed with a MOS transistor biassed in a weak inversion region was addressed by Eric A. Vottoz and colleagues (1977). They examined methodologies, limits, and future potential for creating a low-power circuit. It is covered in detail several of the essential CMOS circuits, such as the low input voltage current mirror, the adaptively biassed differential pair, and the symmetrical inverters in weak inversion areas, as well as their advantages and disadvantages. In addition, as a guideline, an in-depth examination of the various design restrictions for the circuits in question is supplied as well. In addition, the design restrictions of a low power digital circuit are used to demonstrate the use of a weak inversion MOS for low power digital circuit design. As a whole, this research lays the groundwork for the widespread use of a weakly operated MOS for the design of mixed signal circuits in CMOS processes with sub-micron resolution.

Using a weak inversion approach, Troy Stockstad and colleagues (2002) have developed a rail-to-rail low voltage complementary metal oxide semiconductor amplifier. The transconductance of the amplifier is generated by a bulk driven PMOS input stage, which is implemented in the amplifier construction. As a source follower, a depletion type NMOS transistor is employed to drive the majority of the PMOS input stage's output transistors. The unusual combination of a depletion mode source follower and a bulk driven PMOS input stage, in addition to the ability to produce rail-to-rail input for an amplifier, allows for greater design freedom. Additionally, an output stage is presented that has the potential of driving a significant amount of output current in a low voltage environment. The amplifier has a dc gain of 70 dB and a driving current of 30uA at 0.9V supply voltage and a load resistance of 1Mohm [54].

Jaime Ramrez-Angulo et al. (2003) show low voltage analogue circuits based on QFG MOS transistors, which they developed themselves. In general, the functioning of a multi-input FG MOS circuit is characterised by its extremely low voltage. However, this comes at a cost in terms of greater silicon area and lower transconductance, both of which reduce the frequency at which analogue circuits achieve unity gain. Additionally, the FG MOS provides a high offset voltage as a result of the charge entrapment in the floating gate that occurs during the manufacturing process. This work describes a novel family of low voltage analogue circuits based on the QFG MOS idea, which maintains the circuit's unity gain frequency without reducing the circuit's performance. In QFG MOS, the gate terminal is only weakly coupled to one of the power rails with the use of a resistor with a very big value. For the purpose of testing the validity of the suggested concept, a CMOS mixer circuit is designed and constructed as a prototype in 0.5um process utilising a QFG MOS. Input signal swing for a MOS is 0.7V, and the circuit has 0.67V threshold voltage at 0.8V supply voltage, according to the circuit design [96].

Jaime Ramrez-Angulo and colleagues (2004) investigate an additional set of analogue circuits that make use of a QFG MOS transistor that runs at a very low supply voltage. The QFG MOS transistor was the subject of this research, which covered both theoretical and practical features of the device. Additionally, the utility of the QFG transistor is used to produce rail-to-rail output voltage in feedforward and feedback circuit implementation at extremely low supply voltage using a feedforward and feedback circuit design. It is possible to create a variety of low-voltage CMOS circuits, such as analogue switches, programmable-gain amplifiers (PGAs), mixers, track and hold (T/H) circuits, and digital-to-analog converters, for rail-to-rail

output voltage. The aforementioned circuits are developed and built in a 0.5um CMOS process and experimentally confirmed at 1.5V supply voltage with a 20uA biassing current to demonstrate the utility of the suggested technique [97] to demonstrate the feasibility of the proposed approach.

Ravi Chawla and colleagues (2007) have developed a programmable Gm-C filter based on a FG MOS transistor. This work investigates two different types of programmable floating gate OTAs, which are employed for the development of second order low pass and bandpass Gm-C filters, respectively. In order to meet the low voltage requirement, the Gm-C filters are implemented employing operational OTAs that operate in the sub-threshold range. The use of the FG transistor in the OTA accomplishes two tasks: first, it broadens the input range, and second, it cancels the offset voltage through the use of a programmable differential pair.

(2008) suggested a second order Sigma-Delta modulator with 10-bit resolution and low power consumption (140nW at 1.2V over 25Hz bandwidth), which was implemented in a CMOS process and used just 140nW power. The modulator under consideration is primarily intended for use in electroencephalogram applications. In order to accomplish low voltage functioning, the QFG-based circuit is utilised. An amplifier of type AB is used in the modulator; this amplifier works in a weak inversion zone, allowing for extremely low power usage. The simulation results demonstrate that the circuit is suitable for use in a very narrow bandwidth range and that it has an energy efficiency of 1.6pJ per quantization level [26], which is quite high.

An example of a differential voltage follower driven by bulk transistors is shown by S. Vlassis and colleagues (2009). For the same purpose, bulk driven transistors are used in place of a transconductance element to get the same result as using a transconductance element. A few of the most important properties provided by this voltage amplifier include the rail-to-rail output voltage, a very minimal common-mode change in both the input and output, and a constant differential gain value at unity frequency. When the circuit is developed and validated, it is done so with the use of a conventional 180nm CMOS process that operates at a 1V supply voltage and is implemented in a conventional 180nm CMOS process.

This theory was advanced by George Raikos and colleagues (2010), who hypothesised that a bulk-driven fully differential amplifier design would enable great performance to be achieved by operating at a supply voltage as low as 0.8 volts. When using the recommended architecture, a positive feedback loop is integrated into the input stage of the amplifier, which serves to increase the inherent body transconductance of the amplifier. The use of positive feedback loops allows you to increase the voltage gain of an amplifier while simultaneously decreasing the true transconductance of the input stage, as shown in the diagram below. In light of the fact that the bulk-driven input stage transistors are a component of the positive feedback loop, the proposed topology is particularly appealing due to the significant increase in effective transconductance that results as a result of this. A larger rail-to-rail common mode range and a greater noise margin are found in the bulk driven input stage as compared to the conventional input stage, which is more expensive. It was completed in a conventional 180nm n-well CMOS process, with a supply voltage of 0.8V that was optimised, and the amplifier architecture was tested and validated before being put into production. Also evaluated at 0.7V is the circuit, and the results show that it has improved power efficiency over the previous version. When operating at 100 kHz, the amplifier has a voltage gain of 56 dB, an input noise of

154 nV/sqrt(Hz), and a CMRR of 80 dB, all of which are excellent performance characteristics. The amplifier has a current consumption of 130uA and a voltage gain of 56 dB, and it is designed for low-power applications.

Authors Juan M. Carrillo et al (2010) propose a common-mode feedback (CMFB) circuit for a totally differential amplifier, in which they apply four low-voltage topologies to achieve their goal of providing common-mode feedback, according to the authors. Complementary feedback circuit accuracy in totally differential amplifiers is critical to achieving their primary advantages of wide dynamic range and harmonic suppression. The bulk driven MOS transistor is used in the construction of the proposed CMFB circuits since they are designed to function at low voltage, as shown in Figure 1. When a bulk driven MOS transistor is used to drive the output common mode voltage of a completely differential amplifier, it may be possible to set the common mode voltage at the midway of the supply voltage. The circuit may function at a lower supply voltage than would otherwise be feasible with a typical capacitor-based feedback circuit, which would otherwise be impossible. A number of bulk driven common mode detectors with good linearity and suitable for low voltage operation have been shown and proved to operate successfully with the suggested topologies.

YELIN LI and colleagues demonstrated in 2010 that it was possible to increase the transconductance of the RFC OTA while concurrently decreasing the power and area consumption of the antenna. Because it distinguishes between the AC and DC current channels, the RFC OTA may function at a better power efficiency when the Improved Recycling Structure (IRS) is used in conjunction with it. In order to demonstrate the capabilities of the suggested technique, it was designed and implemented using a 0.13um CMOS process with a 1.2V supply voltage in order to demonstrate its capabilities. A CMOS process with a 0.13um pitch was used to fabricate the FC, RFC, and IRFC for the aim of showing the capabilities of the suggested methodology. According to the simulation findings, when comparing the proposed technique to the FC and RFC structures, the results reveal that it results in an increase in GBW of around 230 percent and 60 percent, respectively, when compared to the corresponding FC and RFC structures. As demonstrated in Table 1, the FC and RFC structures both outperform the FC structure in terms of DC gain when the FC structure is used as a comparison structure. When the IRS structure is adopted, on the other hand, it has the consequence of reducing the phase margin of the OTA structure, which is undesirable.

By combining two separate FG and QFG MOS transistors with each other, Christopher Urban and his colleagues (2011) make use of a CMOS transconductor that is rail-to-rail adjustable, which they invented themselves. Transconductance amplifiers with a highly linear broad input range and low supply voltage operation are in great demand owing to their low cost and high efficiency. They are also in high demand due to their low cost and high efficiency. Due to the fact that they are extremely energy efficient and require very little electricity, this is the case. Therefore, the authors used MOSs such as the FG and QFG MOSs, which were designed to minimise the drawbacks of previously published procedures such as adaptive biassing, nonlinearity cancellation, resistive degeneration, and other similar techniques. MOS transistors such as the FG and QFG are also discussed in this chapter, as well as how they may be used in the design of rail-to-rail input stages, transconductance adjustment, and class AB operation, among other things. Linearized triode transistors, which are available in both class A and class AB configurations with output

current scaling, are also discussed in detail in this chapter. The suggested transconductor structures are realised utilising a 0.5um CMOS technology, and the experimental results indicate that the proposed technique is applicable.

A method for boosting the DC gain of a recycling folding cascode optical amplifier by improving the output resistance was proposed by the researchers Xiao Zhao and colleagues (2011). In order to raise the effective output resistance of the cascode load, positive feedback can be utilised to increase the DC gain of the cascode load without reducing the bandwidth of the OTA receiver. With a 1.2V power supply, the suggested amplifier is created and modelled on a 65nm CMOS technology, and it is intended for usage in wireless communications applications. By decreasing the output voltage swing, the simulation results reveal that the gain over the original structure increases by 35.7dB when the original structure is compared to the decreased output voltage swing.

After Yan Zushu, who devised the technique in order to increase the transconductance of the inductively coupled field-effect transistor (IRFC) optical amplifier, they named it the "double recycling technique." Instead of using the conventional input stage, an extra current mirror is used to reuse the current from the shunt path provided by Y.L.Li in the IRFC OTA, and a triplet is recommended in place of the usual input stage of the IRFC OTA, rather than using the conventional input stage. According to comparisons with the FC, RFC, and IRFC structures, this modification in the IRFC OTA indicates the beginning of a new phase of performance improvement in comparison to the other three structures previously analysed. The design and execution of this device were carried out in the 65nm CMOS process at 1V, with the suggested DRFC OTA acting as the foundation for its development and implementation. Based on the simulation results, it is determined that, when compared to the FC structure, the recommended modification to the IRFC OTA results in an approximately 350 percent increase in GBW, while the FC structure results in a 250 percent increase in GBW while maintaining the same power and area budgets. However, as a result of this upgrade, the DRFC OTA has recently been suffering stability concerns.

According to Fabian Khateb et al. (2012), a significant advancement has been made in the utilisation of the QFG MOS transistor for the construction of an ultra-low power current conveyor circuit that operates at a very low supply voltage. In this study, the author analyses and presents a comprehensive review of the QFG MOS transistor, including its potential for use in the construction of a second-generation current conveyor circuit, as well as its shortcomings and drawbacks (CCII). When considering a folded cascode OTA built on CCII with their features, which makes use of a CCII with their features -based QFG as a starting point, we see that non-ideal outcomes might arise that are not ideal. Presented in this work is a current mode quadrature oscillator, which has been developed and tested. It serves as an example of how the CCII may be used in low voltage and low power applications. The suggested circuit runs at a very low supply voltage of 0.4V and requires just 9.5uW of power, making it suitable for low-power applications such as LED lighting. It also has rail-to-rail output swing. CMOS technology with a 180nm pitch was used to achieve the simulation results, which resulted in the output of the desired outcomes.

Positive feedback was employed by Xiao Zhao and colleagues (2012) to increase the transconductance of an OTA while concurrently minimising the power and space needs of the device. The positive feedback technique, when compared to the performance of the RFC OTA while utilising a negative feedback strategy,

greatly improves the performance of the RFC OTA in terms of DC gain, GBW, and slew rate, according to the results of the experiments. In contrast, the improvement in performance comes at the expense of a significant reduction in phase margin (see Figure 1). Results of the structure's design and modelling were released after they were carried out using a 65nm complementary metal-oxide semiconductor process operating at 1.2V supply voltage. It has been demonstrated in both theory and practise that when compared to the normal FC structure, the new structure displays a 400 percent increase in transconductance. Because of this, when comparing the structure to the normal FC structure, the gains are 16.6dB and 8.3dB more than the gains obtained by using the FC and RFC equivalent structures, respectively.

The supply voltage of a bulk driven amplifier is 0.5V, according to Tomasz Kulej (2013), and the amplifier runs at this value when it is turned on. Consider the author's approach to the input stage in comparison to that of the conventional bulk driven amplifier. This approach enables the author to achieve more voltage gain while also providing a broader output swing. Because of the use of a suggested input stage, the three-stage amplifier with the Miller compensation scheme may be implemented at a very low supply voltage of 0.5V, resulting in electrical characteristics that are adequate for this application. By including an input stage, not only is the voltage gain enhanced, but the common mode levels at the input and output are also as close to the midsupply levels as is reasonably practicable without sacrificing performance. The biassing voltages of the amplifiers in many low-voltage classical gate-driven amplifier circuits must be controlled by an additional circuit in order for the amplifiers to operate properly. In this particular instance, the need for such a circuit is no longer necessary. The design and modelling of amplifier architectures were made possible by the use of 50nm CMOS technology and an ideal supply voltage of 0.5V, respectively. A 20pF load capacitor allows the amplifier to attain a 74dB open loop gain while also providing a maximum gain bandwidth of 4.8MHz for the amplifier.

In honour of Bhawna Aggarwal and colleagues (2013), who built a cascode current mirror circuit that had a low voltage and high swing by expanding the use of the bulk driven MOS transistor, they named their circuit the cascode current mirror circuit. When compared to a typical current mirror circuit, the author's self-biased cascode current mirror circuit runs at a lower supply voltage, provides a broader bandwidth, and has a lower output resistance while retaining a lower supply voltage. When comparing the performance of the recommended structure to that of the old structure, the use of an analytical technique was employed to demonstrate the improvement in performance. It has been proven that when 0.25um CMOS technology is used, both the traditional circuits and the suggested circuits work satisfactorily at voltages of 0.75V and 0.5V, respectively, when 0.25um CMOS technology is used. When compared to the standard circuit design, the observed results of computer simulations reveal that the proposed modifications result in greater output resistance and bandwidth at the expense of a slightly increased input resistance, which limits operating range.

Conclusion

The OTA topology plays vital role in designing a low voltage low power application. Although, multistage amplifier gives advantages such greater gain, railto-rail output voltage swing and improved noise tolerance but still nowhere equal the speed and power efficiency of single stage construction. The above study demonstrates that the RFC OTA requires only half the power compared to Telescopic and FC OTA to

perform equally and consequently best appropriate for low voltage low power application. The asymmetrical current splitting in the input stage of RFC OTA demonstrates a considerable boost in the performance of the RFC OTA. The increase is obtained without compromising the power budget of the RFC OTA circuit. The measurement result validates the transconductance increase and detected 520 percent and 13.7 dB boost in GBW and DC gain correspondingly over the traditional FC OTA. Also, the simulation result confirms the ability of the proposed OTA to act as a tunable OTA merely by altering the voltage source. The employment of a positive feedback approach considerably boosts the transconductance of a super class AB RFC OTA which results in enhanced gain, GBW and slew rate. The proposed RFC OTA exhibits a 450 percent improvement in the 92 transconductance findings with about a 13dB spike in gain as compared to the FC OTA. The tradeoff present between the transconductance improvement and phase margin degradation in IRFC OTA may be overcome by dipropionate current splitting in the input stage of IRFC OTA.

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